which was a continuation of Application No. 07/708,099, filed May 24, 1991, now abandoned; which was a continuation of Application No. 07/374,896, filed Jun. 30, 1989, now abandoned.

Delete the section "BACKGROUND OF THE INVENTION" and insert the following replacement section:

BACKGROUND OF THE INVENTION

Traditionally, expensive test equipment has been required to dynamically monitor the functional interactions of integrated circuits on a circuit board design. During test, the integrated circuits are made to operate together functionally while an external tester observes the transactions occurring between the integrated circuits. Other techniques such as boundary scan provide off-line or static testing of wiring interconnects between integrated circuits, but are not effective in detecting at-speed functional problems that can occur in the bussing paths between integrated circuits.

The ability to dynamically (i.e., during normal operation of the circuit board) observe the data passing between integrated circuits in real-time allows monitoring of the functional interactions between multiple integrated circuits on a substrate, such as a circuit board. Such a test can reveal timing sensitive and/or intermittent failures that would otherwise not be detectable without the use of expensive testers and mechanical probing fixtures. The ability to dynamically observe system data buses in real-time facilitates system integration, environmental chamber testing, remote diagnostic testing, and built-in self testing.

Heretofore, the ability to dynamically observe digital signals on buses formed of leads on the substrate or circuit board between integrated circuits has been unavailable. Current test methods used to monitor or observe digital signals on signal paths or leads between integrated circuits on substrate or circuit board designs require the use of expensive external tester equipment and signal node probing mechanisms. One problem with the current test approach is that state-of-the-art circuit board designs are so densely populated with integrated circuits that physical probing of the signal paths is very difficult, if not impossible. Another problem is that the circuit board tester is dependent upon the availability of external testers and probing fixtures. Transportation and upkeep

of the required test equipment in a field environment to support a system can be a very expensive proposition.

Therefore, a need has arisen to provide a digital bus monitoring device which can be used to dynamically observe data or address signals on a bus leads connecting multiple integrated circuits.

Delete the section "SUMMARY OF THE INVENTION" and insert the following replacement section:

SUMMARY OF THE INVENTION

In accordance with the present invention, a digital bus monitor is provided which substantially eliminates or prevents the disadvantages and problems associated with prior digital bus testing devices.

The digital bus monitor of the present invention may be used to observe data on a bus connecting multiple integrated circuits while the integrated circuits are in a functioning mode. Input circuitry is provided for receiving incoming data. Test circuitry is connected to the input circuitry for analyzing and storing data in response to detection of a ~~predetermined~~ known or certain condition. The ~~predetermined~~ known or certain condition may be detected by comparing data from the logic circuitry to an expected data word stored in a register or memory. Some bits of the expected data word may be masked using a masking data word, such that the masked bits are not involved in the matching operation. Multiple digital bus monitor devices may be cascaded together to allow for observation and test of variable width data buses.

The digital bus monitor of the present invention provides several technical advantages over the prior art. The digital bus monitors of the present invention may be imbedded in the circuit board or substrate design and can be activated throughout the life cycle of the substrate or circuit board, from production testing to field service and maintenance. Another advantage is that the digital bus monitors do not impede the performance of the substrate's or board's circuitry. Since the input signals to be monitored do not have to be routed through the digital bus monitor, but are only input

to the digital bus monitor, no significant functional performance penalty is paid while using these devices.

In the second embodiment of the present invention, a second ~~predetermined~~ known or certain condition may be detected, at which time the storage and analysis will cease. The storage and analysis may be resumed after detection of a third ~~predetermined~~ known or certain condition and stop after the detection of a fourth ~~predetermined~~ known or certain condition.

The digital bus monitor of the present invention provides the advantage of analyzing signals or data on data or address buses coupling multiple integrated circuits while the integrated circuits are operating at-speed. The at-speed testing of the integrated circuits detect errors that might not otherwise be found.

Delete the section "Digital Bus Monitor Application" and insert the following replacement section:

Digital Bus Monitor Application

FIG. 1 illustrates a block diagram of an exemplary circuit using the digital bus monitor (DBM) of the present invention. As illustrated in FIG. 1, two integrated circuits, IC1 10 and IC2 12, are connected by three buses: An address bus 14, a data bus 16, and a control bus 18. Each bus is formed of plural leads affixed to a substrate, such as a circuit board. A first data bus monitor DBM1 20 is connected to the control bus 18 by its clock or CK input and to the data bus 16 via its ODI (observability data input) input. The second data bus monitor DBM2 22 is connected to the control bus 18 via its clock CK input and to the address bus 14 via its ODI input. DBM1 20 and DBM2 22 are interconnected together via a serial scan path connection comprising a test data input (TDI) and a test data output (TDO). The TDO of DBM1 20 is connected to the TDI of DBM2 22. Control for operation of the DBMs 20 and 22 for scan and off-line test operations is input via the test clock (TCK) and test mode select (TMS) inputs. The TDI, TDO, TCK and TMS scan path signals are compatible with a proposed IEEE standard test bus for integrated circuits. An event qualification output (EQO) is output from each of the DBMs 20 and 22 into an AND gate 24. The output of the

AND gate 24 is input to the event qualification inputs (EQI) of each DBM 20 and 22. TMS/TCK and TDI may be supplied by an external test bus controller 25. TMS/TCK and TDI may optionally be input to an IC with internal test circuitry. TDO and EQI are received by the test bus controller from DBM2 22 and AND gate 24, respectively.

In operation, the DBMs 20 and 22 are used to observe and test the digital signals carried on the buses 14-18 connected between the two integrated circuits 10 and 12. DBM devices operate in two modes: off-line test mode and on-line test mode. In the off-line mode, board circuitry is placed in a test mode and control for signal monitoring is input to the DBMs 20 and 22 from the external test bus interface. The external test bus interface includes four signals: TCK, TMS, TDI, and TDO. TCK and TMS are the test clock and test mode select signals, respectively, from the external test controller. TDI and TDO are the serial test data input and output signals used to connect DBMs and other devices conforming to the IEEE interface specification. Using the on-line mode, the board circuitry is functioning normally, and control for monitoring comes from the DBMs internal event qualification module (EQM) which is described in detail in connection with FIG. 7.

In the exemplary circuit of FIG. 1, IC1 10 outputs address and control signal information to IC2 12 to allow data signals to pass between the two integrated circuits. First and second DBMs 20 and 22 are included in the circuit of FIG. 1 to ~~allow~~ provide for monitoring the signals on the data and address paths or leads between IC1 10 and IC2 12. The address and data bus signals to be monitored are input to the DBMs via ODI ~~signals~~ leads. If the DBMs were not included in the circuit example of FIG. 1, external probes would have to be connected to these data paths or leads to achieve the level of signal observability provided by the DBMs.

When the circuits ~~is~~ are placed in an off-line test mode, IC1 10 and IC2 12, can be controlled so that the address and data bus paths or leads 14 and 16 can be monitored by the first and second DBMs 20 and 22. During the test, IC1 10 can be made to output data on its address and data buses or leads 14 and 16. The data and address output from IC1 10 can be captured into both DBMs 20 and 22 via ODI 14, 16 inputs. After the data has been captured, it can be shifted out for inspection via the serial scan path from the TDI input pin of DBM1 20 to the TDO output pin DBM2 22.

Similarly, IC2 12 can be made to output data on the data bus leads 16 to be captured and shifted out for inspection by the first DBM 20. In this off-line test mode, control to capture data and operate the scan path is input via the TCK and TMS test bus input pins.

When the circuit of FIG. 1 is on-line and functioning normally, the first and second DBMs 20 and 22 can continue to monitor the data and address buses 14 and 16 using the internal EQM circuitry described below. During on-line monitoring the internal EQM of each DBM device 20 and 22 outputs control signals to capture the data appearing on the ODI inputs of the respective DBMs. The internal EQM operates synchronous to the control signal outputs from IC1 10 which are input to each DBM via the clock or CK inputs. To know when to capture data, the EQM circuitry within each DBM 20 and 22 has comparator logic which can match the data appearing on the ODI inputs against a ~~predetermined~~ known or certain expected data pattern or set of expected data patterns.

To expand the event qualifying capability, multiple DBMs (or other devices containing the EQM and the EQI and EQO pins) can be connected together on an external combining network, such as AND gate 24, to allow the qualification of a test monitor operation to be controlled by the events detected over a range of DBM devices. When expanded qualification is required, each DBM outputs a match condition signal on its EQO output pin. The EQO outputs of multiple DBMs are input to an external combining circuit or AND gate 24 to produce a global event qualifier (EQI) input signal that is fed back into each DBM via their EQI input pins. When a matched signal is input on the EQI pin, the internal EQM can initiate a test monitor operation. The operation and protocol of the Event Qualification Module are described in U.S. ~~patent application Ser. No. 308,272,~~ Patent 5,001,713, entitled "Event Qualified Testing Architecture For Integrated Circuits," and U.S. ~~patent application Ser. No. 308,273,~~ Patent 5,103,450, entitled "Event Qualified Testing Protocols For Integrated Circuits," both filed Feb. ~~9~~ 8, 1989 by Whetsel, both of which are incorporated by reference ~~herein~~ into this patent.

The test bus controller 25 can control the shifting of data through the DBMs (and other devices). The combined EQI signal is monitored by the test bus controller 25 to determine when a known or certain condition occurs. In response to one or more known or certain conditions, the test bus

controller can scan out the data stored in the DBM and other devices. Test protocols and conditions are discussed in connection with FIGS. 7a-d ~~hereinbelow~~.

In the paragraph bridging pages 22-23:

The EQM 32 can perform four types of event qualified testing protocols. Timing diagrams for each of the four types of protocols are shown in FIGS. 7a, 7b, 7c and 7d. A protocol 1 operation allows for performing a single test monitor operation in response to a condition input. A protocol 2 operation allows for performing a test monitor operation while the condition input is present. A protocol 3 operation allows for performing a test monitor operation over an interval of time between a start condition input and a stop condition input. A protocol 4 operation allows for performing a test monitor operation which can be started with a first condition input, paused with a second condition input, resumed with a third condition input, and stopped with a fourth condition input. All the protocols can be made to repeat a ~~predetermined~~ desired number of times as determined by the EQM's internal event loop counter. The operation of the EQM and its protocols are described in detail in U.S. ~~patent application Ser. No. 308,272~~ 5,001,713 and U.S. ~~patent application Ser. No. 308,273~~ 5,103,450, referenced above.

Page 28, the full paragraph:

FIG. 9 illustrates a block diagram of the TCR 28. The TCR 28 includes a register 82 comprised of a series of test cells interconnected to form a test register. The test register 82 is described in detail in U.S. ~~patent application Ser. No. 241,439~~ Patent 5,495,487 to Whetsel, entitled "Testing Buffer/Register," filed ~~Oct. 3~~ September 7, 1988, which is incorporated by reference ~~herein~~ into this patent. Each test cell in the test register 82 is connected to a respective bit (0-15) of the EXPDAT, CMPMSK, DATMSK and ODI signals. The test cell register 82 also receives a PSAENA signal from the command register 36 via the command bus 44 and the output of first, second and third multiplexers 84, 86, and 88. Multiplexer 84 receives the TDI input and an FBO signal. The FBO signal received by the multiplexer 84 is the output of an exclusive or network 90, which is part of the TCR 28. The multiplexer 84 is controlled by the FBSEL signal from the TCR control register 26. Multiplexer 86 has the L/S and TGATE signals as inputs and is controlled by the MODE2

signal from the command register 36 via the command bus 44. Multiplexer 88 receives the DRCK4 and SYNCK signals and is also controlled by the MODE2 signal. The EXOR gate network 90 receives TDO0-15 outputs from the test cell register 82, TAP 0-15 signals, and the output of an AND gate 92. The AND gate 92 receives an FBIENA signal from the TCR control register 26 and the FBI signal. The test cell register 82 outputs CMPOUT signals for each test cell in the register; the signals are input to an AND gate 94 which outputs the CTERM signal. The test cell register 82 also outputs a TDO signal. The number of test cells in the test register is equal to the number of ODI input signals.

In the Claims:

Claims 1-24 (canceled)